Development of ultra-high-speed video cameras for PIV

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Abstract

A series of video cameras of 1,000,000 fps are being developed. The image sensors are the In-situ Storage Image Sensors (ISIS), which have a local memory area within or beside each pixel. During an image capturing phase, image signals are stored in the in-situ memory without being read out of the sensor. During a readout phase after the cease of the image capturing phase, the image signals are slowly read out. The parallel recording operation at all pixels at once achieves ultimate high-speed image capturing. A linear CCD storage placed slightly slanted to the grid of the pixel array serves as the in-situ storage, which makes the structure simple. The simple structure provides more storage capacity within the limited area near each pixel and better image quality with less noise. The sensors are the ISIS-V1 to the ISIS-V3. Example images taken by the ISIS-V1 developed in 2000 are shown. The ISIS-V3 under development has a higher pixel count of a half mega pixels as well as the ultra-high frame rate, which is suitable for high-frame-rate PIV.

1
Introduction

In 1993, a questionnaire was distributed to Japanese scientists and researchers, who were potential users of high speed imaging systems (Etoh and Takehara, 1994). One result was, that the frame rates of available high-speed cameras at that time were not high enough. A camera with a frame rate of 1,000,000 fps and 100 consecutive images would satisfy 95% of the user requirements at that time. In a new questionnaire, distributed in early 2000, users of high-speed cameras requested an even higher frame rate. Now, 10,000,000 fps would cover 92.5% of the applications. To achieve a frame rate of 1,000,000 fps with 100 consecutive images, a concept, the "in-situ storage", is introduced to a high speed CCD image sensor. Each pixel has an own storage area adjacent to the pixel with memory size sufficiently large to reproduce a moving image. This storage is filled with image signals during the image-capturing phase. After the image-capturing phase, the read out of the sensor ensues.

The first successful application of the concept to CCD technology is a burst image sensor with "SPS (Serial-Parallel-Serial) storage" and an overwriting mechanism, presented by late Professor Kosonocky in 1996 (Kosonocky et al, 1996). A camera which uses this sensor is now provided by Princeton Scientific Instruments and has a maximum frame rate of 1,000,000 fps with 32 consecutive frames.

The main problem with this design is the change of transport direction from the serial to the parallel storage. It is necessary to make two direction charge transfer during one integration cycle of the image capturing phase.

To overcome the problem of the direction changes, an ISIS structure with linear storage elements was introduced. The easiest way to produce such a sensor is to apply an additional lightshield to a standard CCD imager. The additional lightshield covers the storage CCD- elements and leaves small openings for the light sensitive CCD elements.

SMD, Silicon Mountain Design, first introduced an ISIS with linear storage to market (Howard, et al. 1997). The camera is now produced by DALSA. It reaches up to 1Mfps with 17 consecutive frames and a resolution of 240x240.

For the first tests of such a structure, the authors developed a camera with a sensor similar to the SMD one. The sensor is called ISIS-V1.

Then, the ISIS-V2 was developed, which has the pixel count of 312x260, the consecutive frames of 104, 50 times higher sensitivity than V1, and the overwriting mechanism, which makes it easy to synchronise timing of image capturing to occurrence of a target event.

Finally, a next-generation image sensor, ISIS-V3, is proposed. The spatial resolution is sufficiently large. The format is originally a half VGA, i.e., 320x480 pixels, and the structure is buttable. Therefore, it can be expanded to a VGA sensor or even to the sensor with the pixel count of 960x480 by triple-butting. The dynamic range (gray level) is 9 bits.

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2
ISIS-V1

2.1 Sensor

The "basis" for the ISIS-V1 is the Philips FXA1012 sensor. This sensor was chosen mainly because the pixels are quite small, 5.1µm x 5.1µm, and it has a full-well capacity of typical 45,000 electrons. It is a frame-transfer sensor using a 4-phase-clocking system and it has a resolution of 1616(H) x 1296(V) pixels.

The lightshield added to the light sensitive area of the FXA1012 is shown in Fig. 1. Below each opened light sensitive pixel, a covered area working as storage for the light sensitive pixel is located. During integration, electrons are collected in the light sensitive pixels and then shifted down into the storage pixels below the light sensitive pixel. Because the FXA1012 is a standard frame-transfer sensor, a drainage of old pixel-information at the end of each storage line is not possible. Integration must stop after the storage line below the light sensitive pixel is filled.

Due to the attached lightshield, the axes of the ISIS image area are not orthogonal, the sensor has to be mounted slanted to the camera. The angle α in Fig. 1 b) is necessary to create squared ISIS-V1 pixels with the maximum fill-factor. The distance between two pixel rows must be the same as the distance between 2 pixel columns, else the image area would be non-rectangular.

For the ISIS-V1, each light sensitive pixel has 16 storage pixels, that means 17 consecutive frames can be taken (16 stored frames + 1 frame in the light-sensitive pixels). The angle of the image section is calculated with formula (1).

a)

b)

Fig. 1: ISIS-V1 punched lightshield, a) location on FXA1012, b) upper right corner

$$\alpha = \arctan \frac{1}{s} = \arctan \frac{1}{4} \approx 14.0° \qquad (1)$$

$$s^2 = 16 : \text{Number of storage pixels}$$

The number of storage pixels is chosen to 16 to create a short movie. The relation between the resolution of the FXA1012 and the ISIS-V1 can be seen in formulas (2) and (3).

$$H = Y + s(X - 1) + R_h \qquad (2)$$

$$V = X + s(Y - 1) + R_v \qquad (3)$$

$H = 1616$: FXA1012 horizontal resolution

$V = 1296$: FXA1012 vertical resolution

$X = 344$: ISIS - V1 horizontal resolution

$Y = 239$: ISIS- V1 vertical resolution

$R_h = 5$: unused pixel column

$R_v = 0$: unused pixel rows

Fig. 2 shows an ISIS-V1 storage line for one light sensitive pixel. The pixel information of different frames for one ISIS-V1 pixel are located in
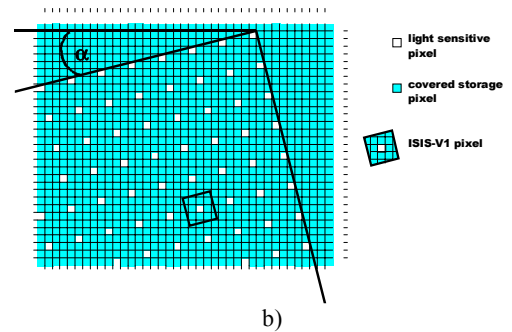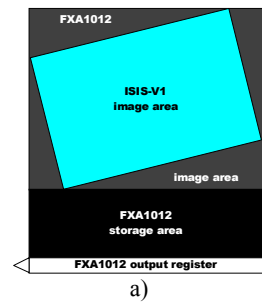

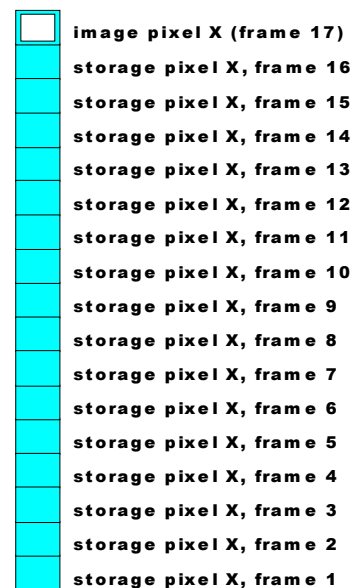| image pixel X (frame 17) |
| storage pixel X, frame 16 |
| storage pixel X, frame 15 |
| storage pixel X, frame 14 |
| storage pixel X, frame 13 |
| storage pixel X, frame 12 |
| storage pixel X, frame 11 |
| storage pixel X, frame 10 |
| storage pixel X, frame 9 |
| storage pixel X, frame 8 |
| storage pixel X, frame 7 |
| storage pixel X, frame 6 |
| storage pixel X, frame 5 |
| storage pixel X, frame 4 |
| storage pixel X, frame 3 |
| storage pixel X, frame 2 |
| storage pixel X, frame 1 |

Fig.2 : ISIS-V1 storage line

the storage column right below the light sensitive pixel (see also Fig. 6).

The opening is chosen to Xμm x Xμm. This is the smallest guaranteed opening in the lightshield due to the production process. Also measurements on a test-sensor, produced before the ISIS-V1, showed that this opening is satisfying to cover the pixels neighboring the light sensitive one. In this test-sensor, openings with different sizes were tested to measure the influence on neighboring covered pixels. The results can be seen in Fig. 3. The test sensor was illuminated and the charge collected in the covered pixels next to a light sensitive one was measured. The neighboring pixels in vertical direction collect much more charge than the ones in horizontal direction. The reason here is that a clock line is located between each FXA1012 pixel column. These clock lines block the light to the left and right next to the light sensitive pixel. There is no such block to the upper and lower pixel. The importance of light blocking to the sides is mainly given during the time the shutter of the camera closes (see B. Camera). In vertical direction, only the first or the last two frames might be over-illuminated, in horizontal direction, frames 4 and 13 might be over-illuminated. Thus, the blocking in horizontal direction is more important because frames from the middle of the movie might become unusable.

2.2 Camera

The camera for the ISIS-V1 must follow a special scheme of integration and read-out, shown in Fig. 4. The normal scheme for an FT-sensor is consecutive integration and read-out. For the ISIS-V1, a start signal has to be set short time before the target action happens. After that, 16 frames are taken and stored in the storage area below the light sensitive pixel. The speed of the shift to the storage is variable, maximum speed is 1μs (1,000,000 fps). Before read-out ensues, a mechanical shutter has to darken the sensor because it is read out through light sensitive pixels. During the time the shutter closes, the 17th frame is taken in the light sensitive pixel.

After read-out, the pixels have to be sorted to create 17 single pictures (Fig. 6, 7, 8). These pictures then can be combined to a movie.

2.3 Supporting technologies

The shortest integration time for the FXA1012 is recommended 1/120s. If the frame rate of the ISIS-V1 is set to 1,000,000 fps (integration time < 1μs), this sensor needs about 8400 times more light to deliver the same signal. It is necessary to support the camera with a special strobe which has a high intensity and a short tail (to avoid over-illumination during shutter-closing).

2.4 Example Images and Associated Problems

Fig. 5 shows the lower left corner of the complete ISIS-V1 image area. The holes here represent the light sensitive pixels. In Fig. 6, pixel information of that part can be seen. The different frames are quite good visible. A complete ISIS-V1 picture before sorting is shown in Fig. 7. The marked triangular parts at the top of Fig. 7 have light sensitive pixels with different openings in the lightshield and are used only for tests. Fig. 8 shows the sorted 17 frames. The last two frames, 16 and 17, are over-illuminated while the first image is normally illuminated. The flashlight during capturing of this sequence was located lower than the captured object, so the
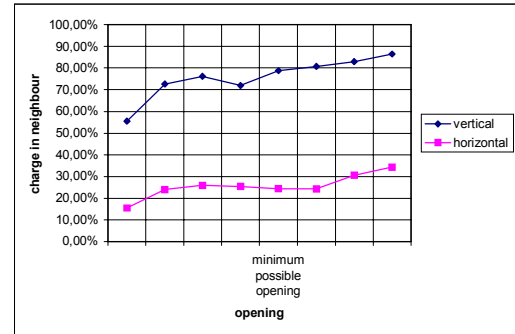

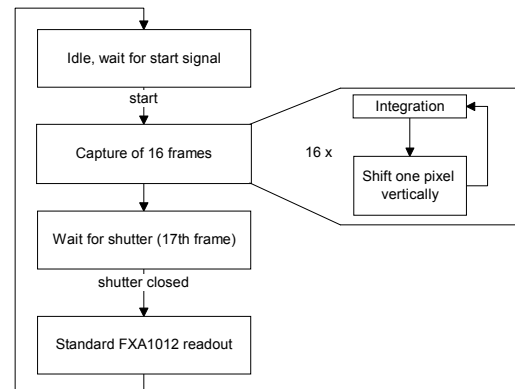
Fig. 3: Charge in covered pixels next to opened ones
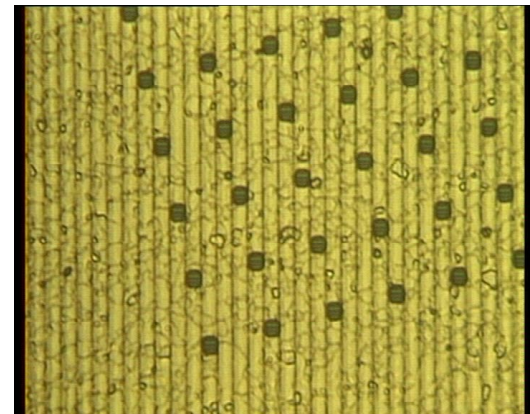

Fig. 4: ISIS-V1 imaging cycle

Fig. 5: ISIS-V1 lightshield with holes (lower left part)

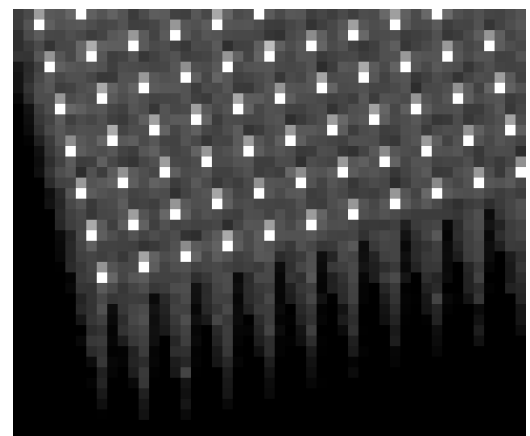Fig. 6: ISIS-V1 image before sorting (lower left part)

16th frame was more illuminated.

The weak points of ISIS-V1 are:
-low light sensitivity
-low fill factor (about 3%)
-small number of consecutive frames
-no overwriting mechanism
To overcome these problems, a new sensor, ISIS-V2, was developed by the authors.

3
ISIS-V2

The lightsensitive pixels in the ISIS-V2 are about 50 times larger than the storage pixels, so they are much more sensitive

and a much better fill-factor is achieved. An overwriting mechanism is added at the end of each storage column. The number of consecutive frames is 105. Fig. 9 shows a scheme of the ISIS-V2, lower left corner. During integration, the storage area is filled up to the overwriting pixel. There, old pixel information is drained. During read-out, a part of the storage pixels act as a vertical register (see Fig. 9b). It is clocked independently from the other storage pixels. The vertical register pixel information is shifted to the horizontal register and then read out, pixel information in the other storage pixels is not shifted during that time. After the vertical register is emptied, it is filled again from the storage pixels and then again read out. This ensues until the sensor is read out completely.

4
ISIS-V3

4.1 Basic Layout

The concept is illustrated in Fig.10 and Fig.11. Fig. 10 shows a pixel, consisting of
(1) a large photogate,
(2) a linear CCD storage,
(3) a vertical readout CCD, and
(4) a double-functioned CCD element (a) for switching between the storage and the readout CCDs and (b) for overwriting drainage.

Fig.11 shows layout of pixels around the center line of the chip.

4.2 Vertical Readout and Switching CCDs

Switching CCD had been proposed by the third author into the ISIS design. It is placed at a confluence of two CCDs at the lower end of a storage CCD and that of a segment of a vertical readout CCD for a pixel.

The CCD transfer scheme is a standard four-phase one, which requires four metal shunting wires to increase the transfer rate. Therefore, introduction of a vertical readout CCD requires additional four metal shunting wires on or along one CCD channel for vertical readout. It
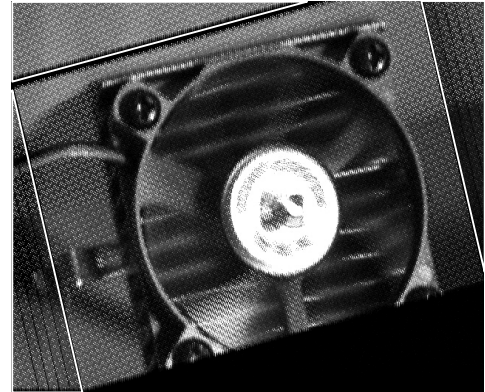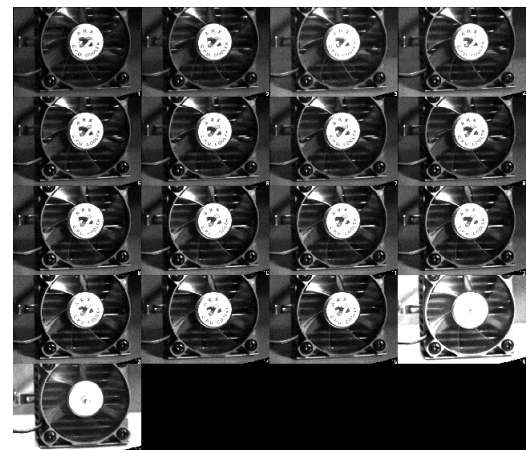

Fig. 7: ISIS-V1 image before sorting

Fig. 8: ISIS-V1 image after sorting

a)   b)

■ Light sensitive pixel

■ Overwriting pixel
□ Storage pixel
□ Vertical read-out pixel
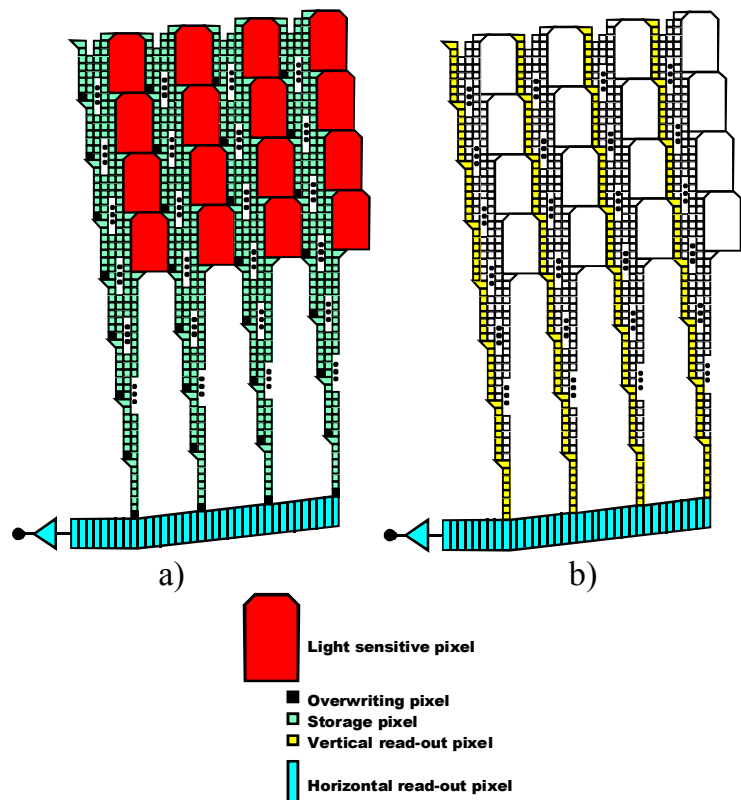
| Horizontal read-out pixel
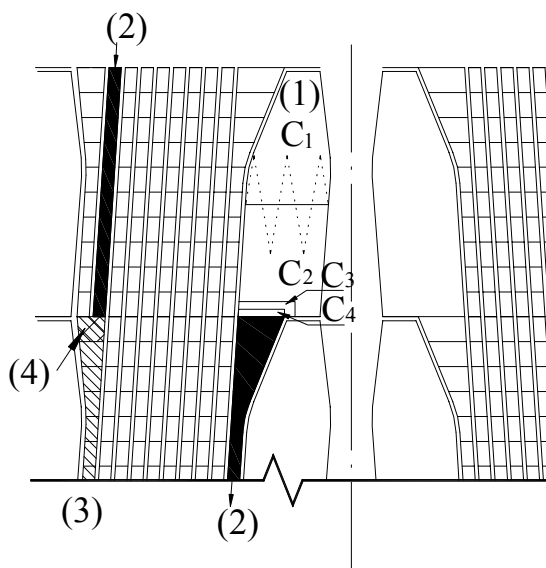
Fig.9: ISIS-V2 sensor scheme a) integration b)read-out

Fig.10: Pixel layout : detail (1) a large photogate (2) a linear CCD storage (3) a vertical readout CCD (4) a double-functioned CCD element (a) for switching between the storage and the readout CCDs and (b) for overwriting drainage

consumes a lot of space, since pitch of shunting wires should be larger than a critical value to keep the yield rate reasonable. An innovative scheme to decrease the number of shunting wires for the vertical readout CCD from four to two is proposed by the second author.

The scheme is conceptually explained in Fig.12.

The linear storage CCD is operated with a set of four electrodes on a CCD element, i.e., A1, A2, A3 and A4, while the vertical readout CCD with A1, B2, A3, B4. Namely, two of four electrodes, A1 and A3, are commonly used, and two additional electrodes, B2 and B4, are placed on the vertical readout CCD instead of A2 and A4.

Transfer voltage patterns for A1 and A3 are always those of standard four-phase transfer as shown in Fig.12 (a).

4.3 Buttable Design

As shown in Fig.11, the storage area can be excluded for the design of mirrored (or rotated) pair of ISISes, which provides a linear wide space at the center of the chip, making the buttable design practical. Together with the increase of the pixel count of the half sensor, the VGA format can be realized for ultra-high speed image capturing.

The pixel size is 50 x 50 square microns. The width of the storage area is about 40 microns, which provides 40-micron space at the center of the buttable design.

4.4 Performance

The size of a storage CCD element is 3 microns x 5 microns, which can be non-square since it is not for Imaging, but only for storage. Charge handling capacity is proved to be about 15,000 by simulation, which provides more than 9 bits in gray-scale for the noise level of 40 electrons.

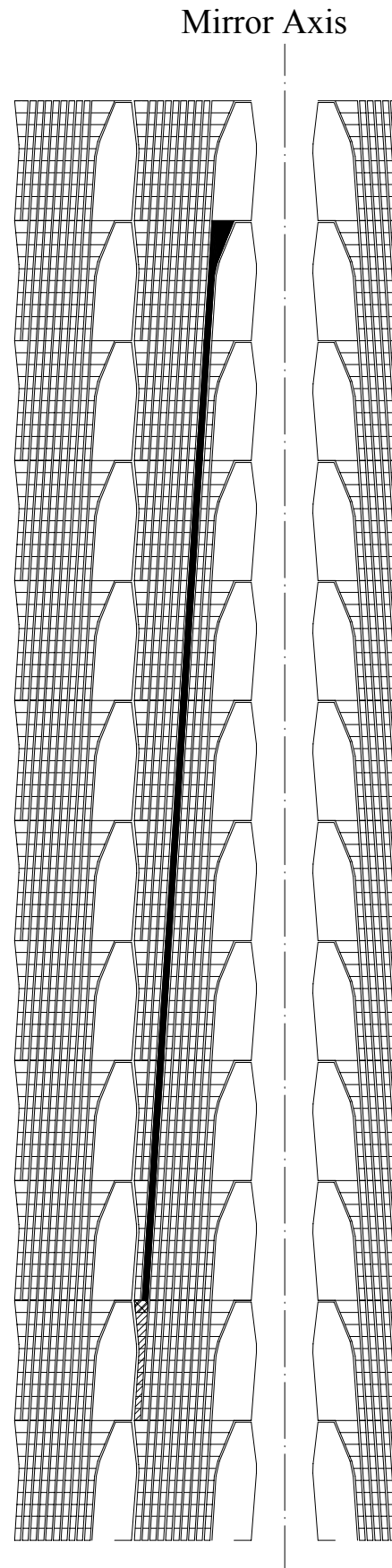The expected performance is tabulated in Table 1.

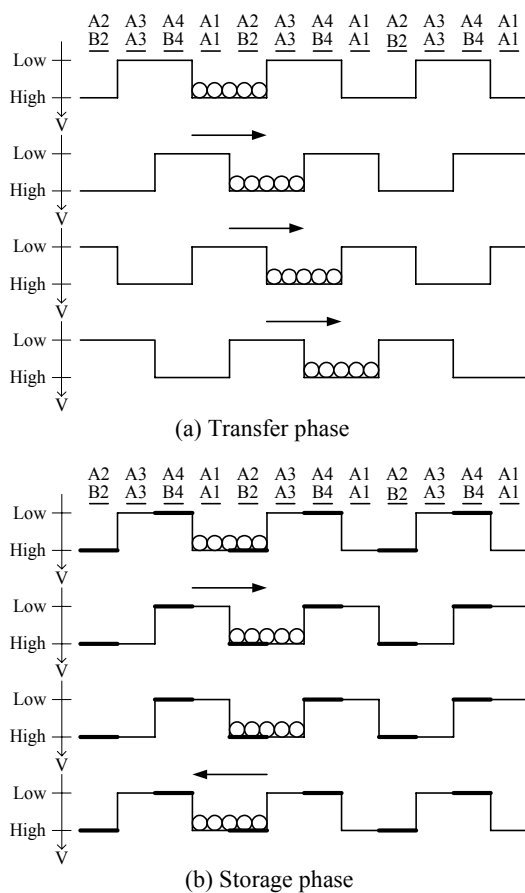Fig.11 Pixel layout around the center line

Table 1: Performance of a proposed ISIS

Basic structure	Buttable ISIS
Pixel count	320x480 (Single Sensor) 640x480 (VGA for Buttable Design)
Number of consecutive images	100 frames
Size of a CCD element	3 microns x 5 microns
Size of a pixel	50 microns x 50 microns
Size of a photo-receptive area of a single sensor	16 mm x 24 mm
Fill factor	20%
Charge handling capacity	15,000 electrons
Grey levels	9 bits
Overwriting mechanism	included

(a) Transfer phase

(b) Storage phase

Fig.12: Operations of two adjacent CCD channels of 4-phase transfer with 6 shutting wires

5 Conclusion

A series of video cameras of 1,000,000 fps are being developed. The image sensors are the In-situ Storage Image Sensors (ISIS), which have a local memory area within or beside each pixel. During an image capturing phase, image signals are stored in the in-situ memory without being read out of the sensor. During a readout phase after the cease of the image capturing phase, the image signals are slowly read out. The parallel recording operation at all pixels at once achieves ultimate high-speed image capturing. A linear CCD storage placed slightly slanted to the grid of the pixel array serves as the in-situ storage, which makes the structure simplest. The simplest structure provides more storage capacity within the limited area near each pixel and better image quality with less noise. The sensors are the ISIS-V1 to the ISIS-V3. Example images taken by the ISIS-V1 developed in 2000 are shown. The ISIS-V3 under development has a higher pixel count of a half mega pixels as well as the ultra-high frame rate, which is suitable for high-frame-rate PIV.

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